In the Abstract:

Please insert the following paragraph on a separate sheet following the claims section beginning on page 12, line 1:

--Abstract

A circuit arrangement for a communication system for terminating a plurality of interfaces at a common bus and for generating a synchronization clock for synchronizing the bus is provided. In one aspect, a circuit arrangement for a communication system includes a first multiplexer controlled by a first control signal with a plurality of inputs corresponding to a plurality of transmission lines of the interfaces, a respective phase control unit, preceding each input of the first multiplexer, which derives a respective clock generator signal from a received signal of the corresponding transmission line, where the clock generator signal of one of the transmission lines is switched through as output signal of the first multiplexer in dependence on the first control signal, and a phase locked loop, at the inputs of which the output signal of the first multiplexer and a clock from a clock generator operated with an external crystal oscillator.--